Ordering number: EN 4092A



No. 4092A

Monolithic Linear IC

LA1862M

Single-chip Tuner System for Car Stereo

OVERVIEW

The LA1862M is a single-chip car stereo FM IF/NC/MPX tuner IC which offers improved IF stability and S-meter characteristics, compared with the LA1861M.

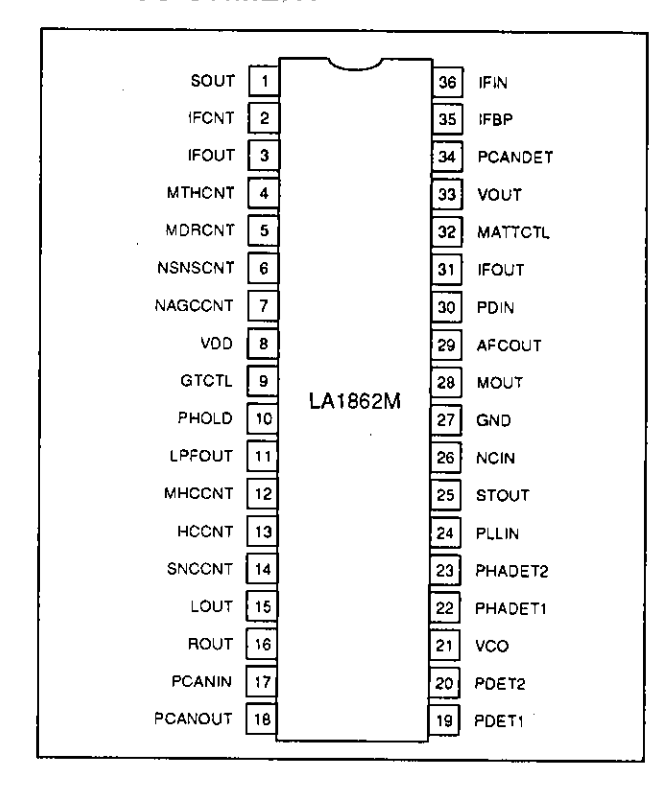
The LA1862M incorporates an IF amplifier, peak detector, AF preamplifier, AFC output, S-meter driver, soft mute circuit, IF buffer output, noise canceller, adjustment-free VCO, pilot signal canceller, high-cut control and SNC on-chip, making the design of high-performance FM tuners easy.

The LA1862M operates from a 7.5 to 10 V supply and is available in 36-pin MFPs.

FEATURES

- Pin compatible with the LA1861M
- Improved I/O S-meter characteristics
- Excellent sound quality at low input levels
- Easy adjustment of muting characteristics
- IF amplifier
- Peak detector
- AF preamplifier
- AFC output
- S-meter driver
- Soft mute circuit
- IF buffer output
- Noise canceller
- Adjustment-free VCO
- Pilot signal canceller
- 7.5 to 10 V supply
- 36-pin MFP

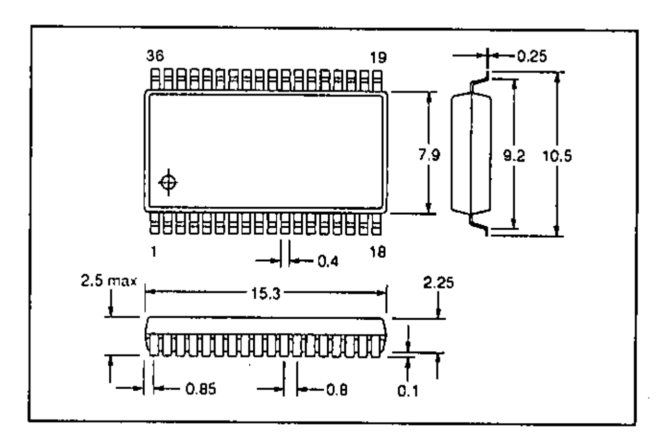
PIN ASSIGNMENT



PACKAGE DIMENSIONS

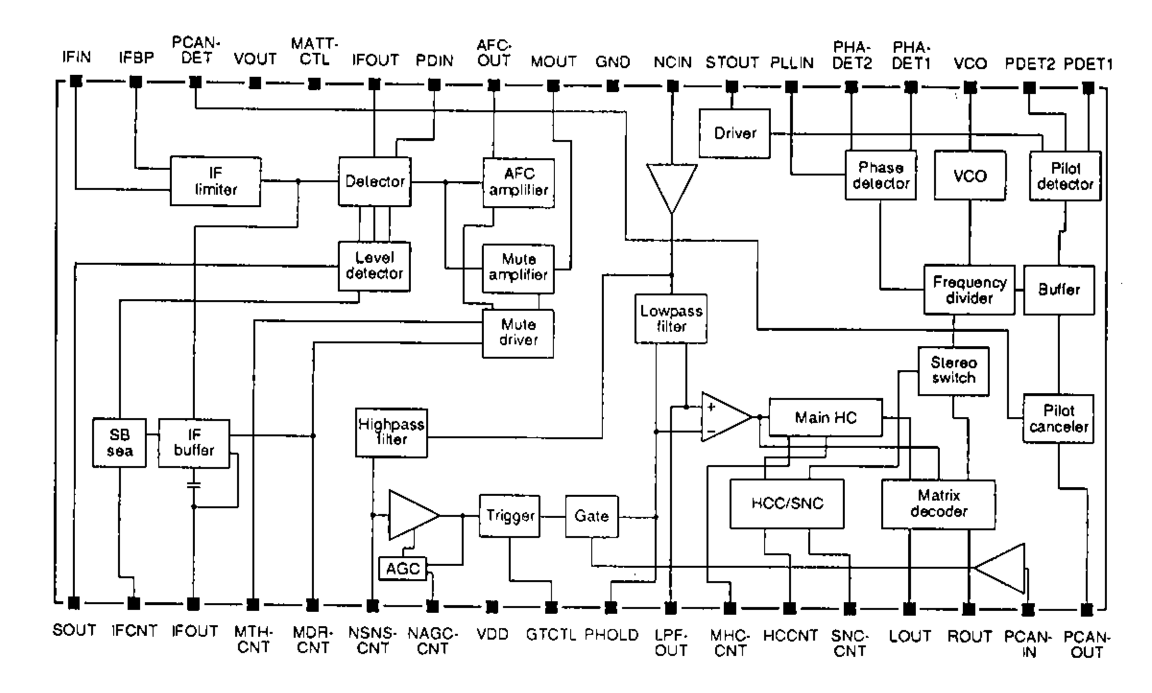
Unit: mm

3129-MFP36S



SANYO Electric Co., Ltd. Semiconductor Business Headquarters
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BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	Description
1	SOUT	S-meter output
2	IFCNT	IF buffer sensitivity control
3	IFOUT	IF buffer output
4	MTHCNT	Muting threshold control
5	MDRCNT	Muting drive control output
6	NSNSCNT	Noise sensitivity control
7	NAGCCNT	Noise AGC sensitivity control
8	VCC	Supply voltage
9	GTCTL	Gate time control output
10	PHOLD	Peak hold network connection
11	LPFOUT	Lowpass filter output
12	MHCCNT	Main high-cut attenuation control
13	HCCNT	High-cut control
14	SNCCNT	SNC control
15	LOUT	MPX left-channel audio output
16	ROUT	MPX right-channel audio output
17	PCANIN	Pilot cancel signal input
18	PCANOUT	Pilot cancel signal output
19	PDET1	Pilot detector capacitor connection 1
20	PDET2	Pilot detector capacitor connection 2
21	VCO	External VCO crystal (F23) oscillator connection
22	PDET1	Phase detector network connection 1

Number	Name	Description
23	PDET2	Phase detector network connection 2
24	PLLIN	PLL input
25	STOUT	Stereo indicator LED driver output
26	NCIN	Noise canceller input
27	GND	Ground
28	MOUT	Audio muting amplifier output
29	AFCOUT	AFC output
30	PDIN	Peak detector input
31	IFOUT	IF signal output
32	MATTCTL	Muting attenuation control
33	VOUT	Voltage reference output
34	PCANDET	Pilot signal canceller detector connection
35	IFBP	IF bypass input
36	IFIN	IF input

SPECIFICATIONS

Absolute Maximum Ratings

T_a = 25 °C

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	10	V
IF input voltage range	V_{IIF}	–0.7 to +0.7	V_{p-p}
NCIN input voltage	V_{IMPX}	1	V_{rms}
Input current	I_I	20	mA
Output current	I_O	1	mA
Power dissipation	P_D	720	mW
Operating temperature range	T_{opr}	–30 to +80	°C
Storage temperature range	T_{stg}	–40 to +150	°C

Recommended Operating Conditions

T_a = 25 °C

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	8.5	V
Supply voltage range	V_{CC}	7.5 to 10	V

Electrical Characteristics

T_a = 25 °C, V_{CC} = 8.5 V, f = 10.7 MHz unless otherwise noted

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Quiescent current	I_{CCO}	No input signal	–	45	70	mA
Operating current	I_{CC}	V_I = 100 dBμ	–	47	72	mA
LOUT demodulator output voltage	V_O	V_I = 100 dBμ, f = 1 kHz, 100% modulation	225	350	495	mV_{rms}
Total harmonic distortion	THD	Mono, V_I = 100 dBμ, f = 1 kHz, 100% modulation	–	0.3	1.2	%
		Stereo (L + R), V_I = 100 dBμ, f = 1 kHz, 100% modulation	–	0.3	1.2	
Signal-to-noise ratio	S/N	V_I = 100 dBμ, f = 1 kHz, 100% modulation	64	71	–	dB
Input limiting voltage	V_{ILIM}	V_I = 100 dBμ reference, 3 dB audio output attenuation, IF input level, soft muting ON, f = 1 kHz, 100% modulation	32	41	50	dBμ
Mute attenuation	α_{MUTE}	V_{MDRCNT} = 5 V, V_I = 100 dBμ, f = 1 kHz, 100% modulation	21	25	29	dB
		V_{MDRCNT} = 2 V, V_I = 100 dBμ, f = 1 kHz, 100% modulation	5	10	15	
Mute bandwidth	BW_{MUTE}	V_{MDRCNT} = 2 V, V_I = 100 dBμ	135	200	305	kHz
AM rejection ratio	AMR	V_I = 100 dBμ, 400 Hz, 100% modulated FM carrier. 1 kHz, 30% modulated AM interference signal	47	60	–	dB
Muting drive output voltage	V_{MDRCNT}	No input signal	3.5	4.7	–	V
		V_I = 100 dBμ	–	0	0.3	
S-meter output voltage	V_{SOUT}	No input signal	–	0.1	0.5	V
		V_I = 50 dBμ	1.1	1.9	2.7	
		V_I = 100 dBμ	5.4	6.4	7.4	
IF COUNT output sensitivity	S_{ICO}	At IF COUNT ON. SW-1 is ON.	44	53	62	dBμ
IF buffer output voltage	V_{IF}	V_I = 100 dBμ. SW-1 is ON.	200	300	480	mV_{rms}
Input impedance	Z_I	f = 1 kHz	–	20	–	kΩ
Output noise voltage	V_{NO}	NCIN connected to ground	–	27	–	μV
Gate time	t_{gate}	V_I = 100 mV_{p-p}, 1 μs pulsewidth, f = 1 kHz	13	23	35	μs
Noise sensitivity	S_N	1 μs pulsewidth, f = 1 kHz	–	–	35	mV_{p-p}

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Channel separation	Sep	f = 1 kHz, 90% L + R signal modulation, 10% pilot signal modulation, IHF bandpass filter	36	50	–	dB
Stereo indicator threshold level	TL_{SI}	Pilot signal level is measured when the LED turns ON.	1.0	2.5	5.0	%
Stereo indicator hysteresis	Hys	LED ON level – LED OFF level	–	3.2	6.5	dB
Capture range	CR	See note 2.	–	±1.2	–	%
SCA rejection	SCA_{rej}	90% L + R signal modulation, 10% pilot signal modulation, 67 kHz, 10% modulated SCA signal	–	75	–	dB
SNC output attenuation	α_{SNC}	V_{SNCCNT} = 0.6 V, 90% L – R signal modulation, 10% pilot signal modulation	–12	–7.5	–3.0	dB
SNC output voltage	V_{Osub}	V_{SNCCNT} = 0.1 V, 90% L – R signal modulation, 10% pilot signal modulation	–	–	5	mV
High-cut control output attenuation	α_{HCC}	V_{HCCNT} = 0.6 V, 90% L + R signal modulation, 10% pilot signal modulation	–15	–5	0	dB
		V_{HCCNT} = 1.1 V, 90% L + R signal modulation, 10% pilot signal modulation	–2.0	–	0	
Ripple rejection	R_{rej}	f = 50 Hz, V_I = 100 mV_{rms}	–	27	–	dB
Channel balance (LOUT – ROUT)	CB	V_I = 100 dBμ, f = 1 kHz (mono), 100% modulation	–	0	1.5	dB
Pilot signal attenuation	α_{PILOT}	Left channel adjusted and measured, DIN audio filter. See note 1.	15	22	–	dB
Stereo indicator LED current	I_{OS}	Minimum stereo drive current	1	–	–	mA
Stereo indicator LED saturation voltage	V_{SAT}	I_L = 10 mA	–	1	–	V

Notes

1. When a filter is not specified, connect an IHF bandpass filter to the audio outputs.
2. The capture range is calculated using the following equation.

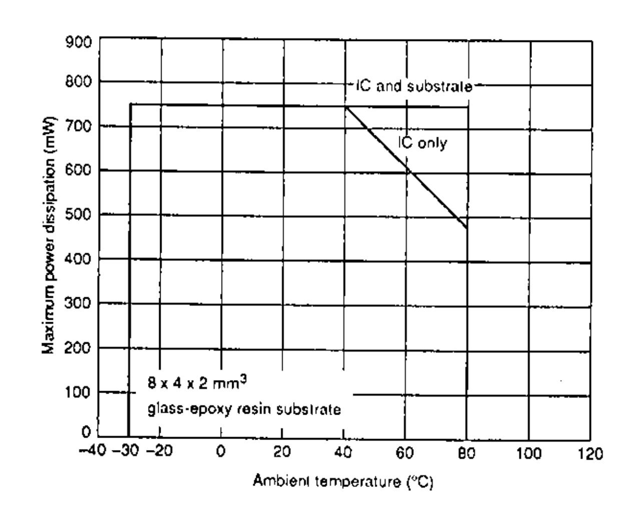
$$CR = \left|\frac{f - 456}{456}\right| \times 100$$

Measurement Circuit

Signal generator
50 Ω
V_DD
NCIN
10 μF
510 Ω
51 Ω
V_DC
V_DD
1 μF
7.5 kΩ
300 Ω
1 μF
10 μF
30 kΩ
1 kΩ
0.22 μF
K41
0.022 μF
3.9 kΩ
4.7 μH
0.022 μF
F23
1 MΩ
51 Ω
1000 pF
100 kΩ
39 pF
10 pF
3300 pF
1 5.6
μF kΩ
2.0 pF
1 μF
330 Ω
0.022 μF
sw-4
IFIN | IFBP | PCAN-DET | VOUT | MATT-CTL | IFOUT | PDIN | AFC-OUT | MOUT | GND | NCIN | ST-OUT | PLLIN | PHA-DET2 | PHA-DET1 | VCO | P-DET2 | P-DET1
36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21 20 19
IF limiter
Detector
AFC amplifier
Driver
Phase detector
VCO
Pilot detector
Level detector
Mute amplifier
Mute driver
Lowpass filter
Frequency divider
Buffer
Stereo switch
SB sea
IF buffer
Highpass filter
Main HC
Pilot canceler
HCC/SNC
Matrix decoder
Trigger
Gate
AGC
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18
SOUT | IFCNT | IFOUT | MTH-CNT | MDR-CNT | NSNS-CNT | NAGC-CNT | VDD | GTCTL | P-HOLD | LPF-OUT | MHC-CNT | HC-CNT | SNC-CNT | LOUT | ROUT | PCAN-IN | PCAN-OUT
0.047 μF
10 kΩ
7.5 kΩ
0.022 μF
51 kΩ
SW-1
5 V
1 kΩ
1 μF
51 kΩ
5.6 kΩ
0.01 μF
22 μF
47 kΩ
47 μF
2200 pF
6.8 kΩ
7.5 kΩ
6800 pF
100 μF
sw-3
0.015 μF
0.015 μF
10000 pF
50 kΩ
0.022 μF
1.1 V
0.6 V
0.1 V
3 V
DIN AUDIO
IHF BPF
DIN AUDIO
IHF BPF
Buffer
SW-2
5 V or 2 V
V_DD

Typical Performance Characteristics

Maximum power dissipation vs. ambient temperature

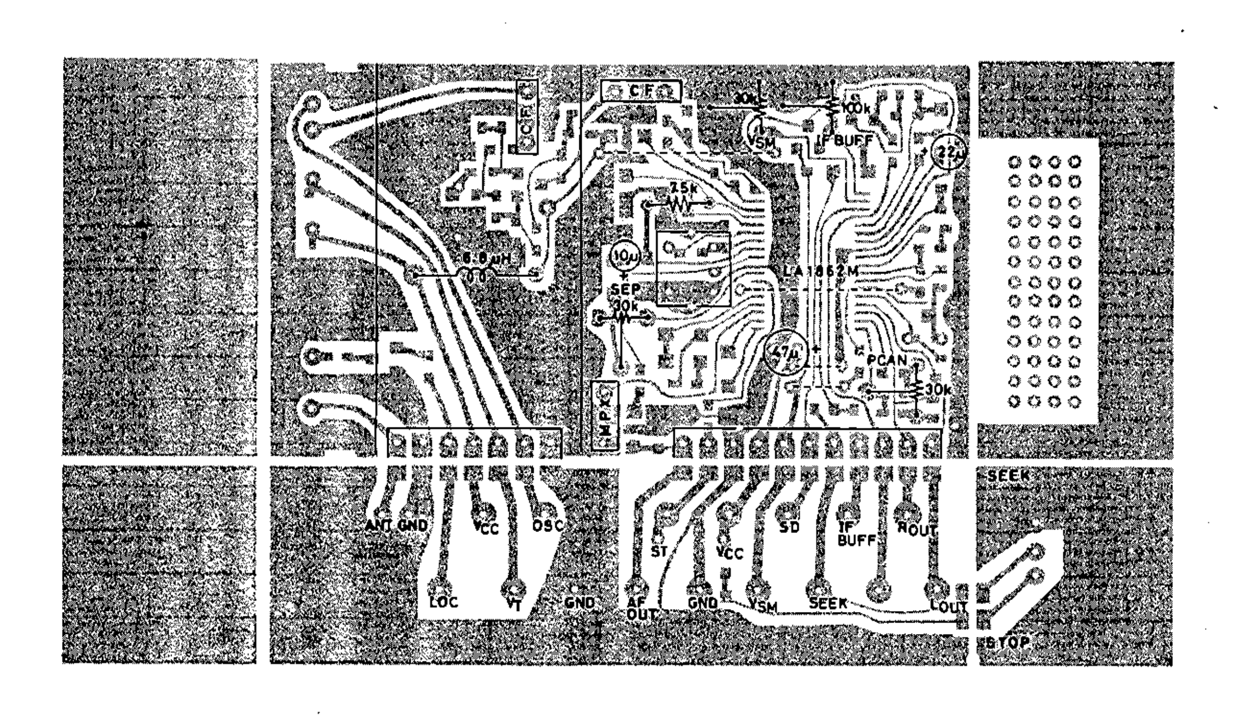


TYPICAL APPLICATION

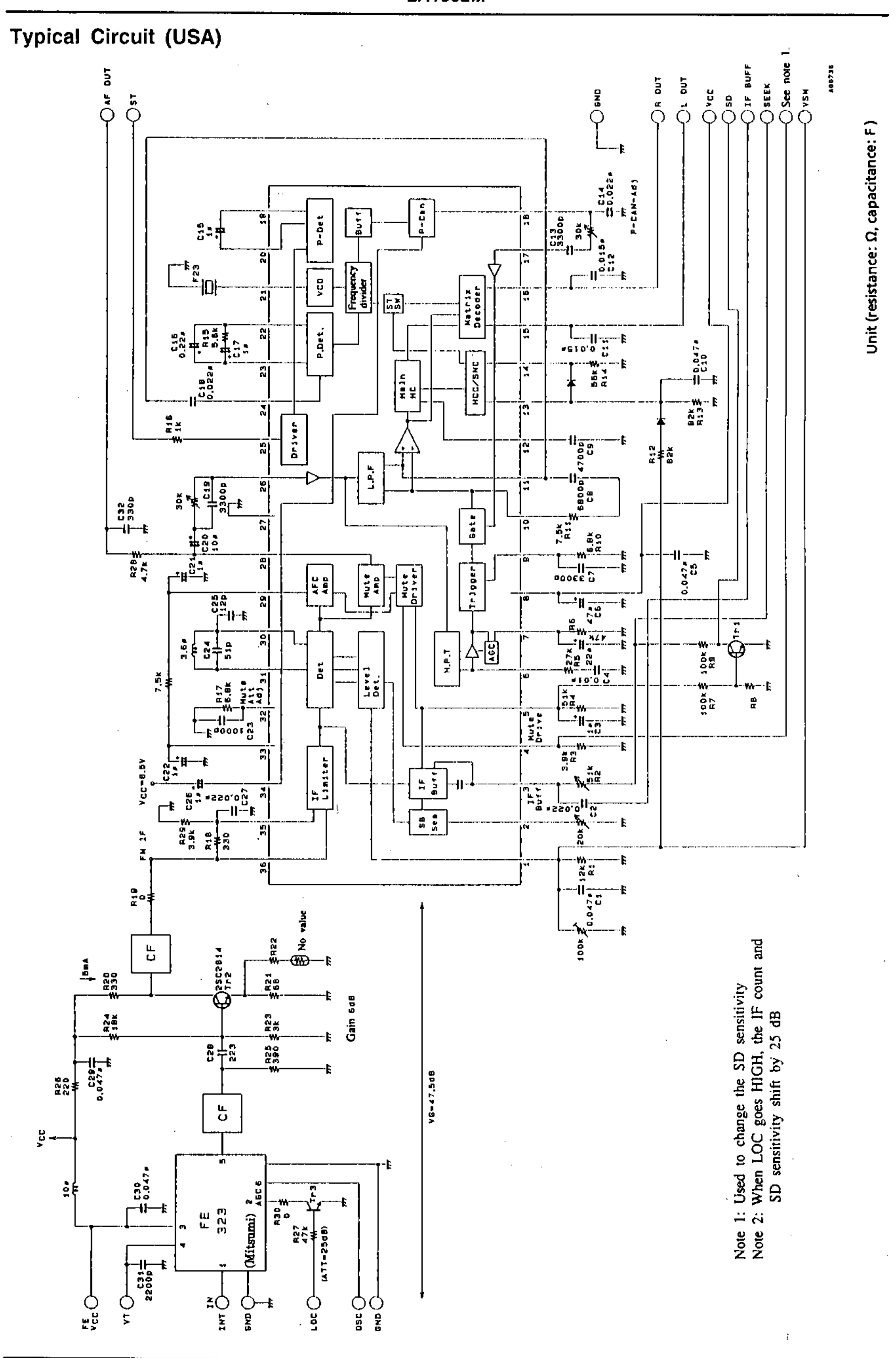
Typical Circuit

Unit (resistance: Ω, capacitance: F)

PCB Pattern



Typical Circuit (USA)



FUNCTIONAL DESCRIPTION

Pin Functions

Unit (resistance: Ω)

Number	Function	Equivalent circuit	Remarks
35	IF bypass		
36	IF input		
1	S-meter output		Current-drive waveform S-meter circuit
4	Mute adjust		
30	Peak detector input		
31	Constant voltage output		

Unit (resistance: Ω)

Number	Function	Equivalent circuit	Remarks
18	Pilot cancel signal output	19kHz, F.F, 5k, 15k, 5k, 15k, ⑱, ㉞	
34	Pilot cancel signal detector		
15	MPX outputs	VCC, ⑮, ⑯, 3.3k, 3.3k, Multiplier	R_{OUT} = 3.3 kΩ Load has built-in resistance
16			
23	Phase detectors	Composite signal, 15k, 5k, 15k, 5k, F.F, 19kHz, ㉓, ㉒	
22			
21	VCO	VCO, ㉑	
20	Pilot detectors	Composite signal, 15k, 5k, 15k, 5k, F.F, 19kHz, ⑳, ⑲	
19			

Unit (resistance: Ω)

Number	Function	Equivalent circuit	Remarks
10	Memory circuit		
11	LPF output		
17	Pilot cancel signal input		
26	Noise canceller input		
12	High-cut capacitive coupling		High-cut frequency set pin
24	PLL input		
2	IF buffer ON adjust		

Number	Function	Equivalent circuit	Remarks
5	Mute drive		
6	Noise sensitivity adjust		
7	Noise AGC		
9	Gate time adjust		The gate is open when the voltage on pin is 1.4 V ($2V_D$) or higher.
33	Constant voltage circuit		

Unit (resistance: Ω)

Number	Function	Equivalent circuit	Remarks
28	Muting circuit output		Z_{OUT} (pin 28) = 50 Ω
32	Muting attenuation adjust		
29	AFC output		
3	IF buffer output		Control signal: SEEK when HIGH (V_{DD}) and STOP when LOW (GND) Pin 3 should be left open if not using the IF count
13	HCC control input		

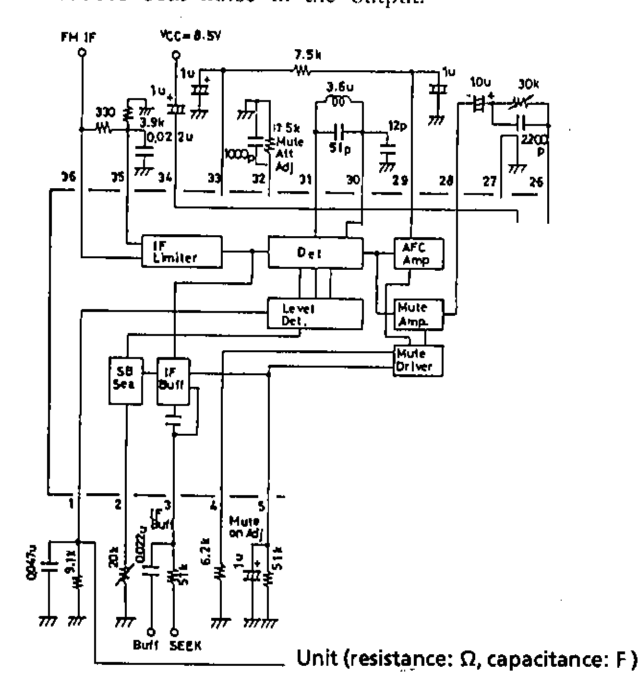
Unit (resistance: Ω)

Number	Function	Equivalent circuit	Remarks
14	SNC control input	5k, 6.8k, (14)	
25	ST indicator	P-Dat, Schmitt trigger, Inversion circuit, (25)	Mono when HIGH and stereo when LOW

IF Block

Obtaining Stable Characteristics

1. Pin 36 is the IF input; pin 35, the IF bypass. Connect a 330 Ω resistor between them for ceramic filter matching.
2. Position the capacitor between the IF bypass (pin 35) and the ground pattern so as to maximize AM rejection.
3. Provide separate ground pattern islands for the IF input and detection circuits, as sharing the same island reduces stability.
4. Position the IF input and detector coil as far apart as possible, as proximity reduces stability and introduces beat noise in the output.



Unit (resistance: Ω, capacitance: F)

S-meter Output V_{SM}

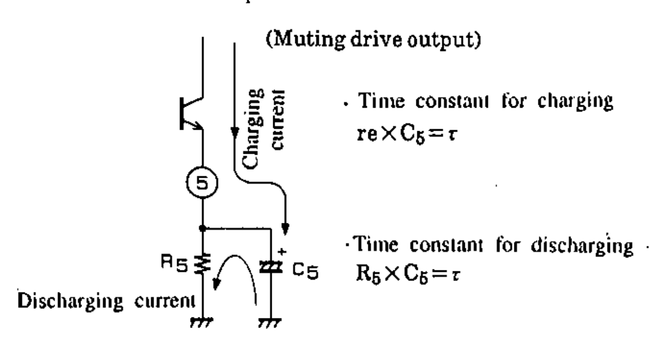
1. Pin 1 is the field strength indicator (or "S-meter") output. Its current-driven circuit uses an external resistance to adjust the slopes of the I/O characteristics curves.
2. The S-meter output is internally connected to the soft muting and IF buffer blocks for use as a control signal for the soft muting drive and IF count buffer.
3. The point at which the input produces an S-meter output depends on the front end (FE) and interstage amplifier gains.
4. Too large a front end gain produces floating S-meter output even when there is no input. Either use a smaller load resistance on pin 1 or reduce the front end gain so that the output with no load does not exceed 0.5 V.
5. The S-meter output circuit has a dynamic range of approximately 80 dB, but this is limited by the front end noise component and broadband AGC circuit.

Soft Muting

1. The soft muting circuit operates in response to the S-meter output voltage. The amount of muting is related to the pin 5 output voltage.
2. There are two mechanisms for adjusting the soft muting I/O characteristic curve:
   a. Start point for muting: Resistance attached to pin 4
   b. Attenuation for muting: Resistance attached to pin 32

   Note that the resistance attached to pin 1 also affects the curve.

3. The soft muting circuit automatically varies the amount of muting in response to the IF input. In the absence of front end broadband AGC effects, the time constant of the RC circuit between pins 1 and 5 determines the response.



Band Muting

1. Band muting uses the detector's S-curve. The bandwidth depends on the resistance between pins 29 and 33. Select this value to match the needs of the destination market.
2. Keep in mind that changing the detector coil or tuning capacity Q changes the slope of the S-curve and hence the bandwidth.
3. The attenuation muting depends on the resistance connected to pin 32.
4. The muting transient response depends on the resistance between pins 29 and 33, the capacitance at pin 29, and the time constant for the RC circuit at pin 5.

Detector

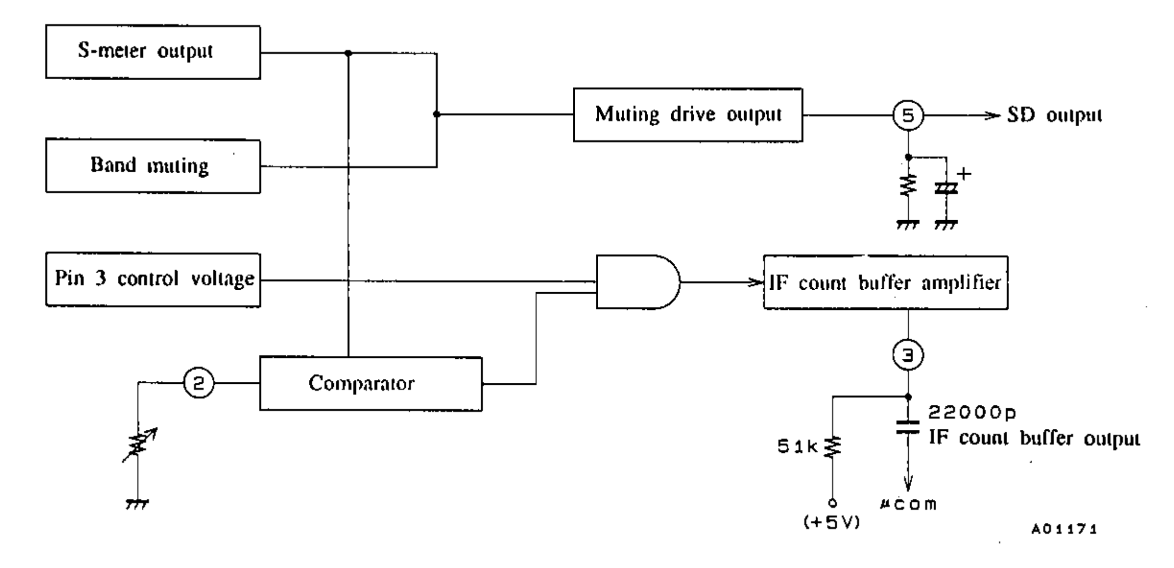
1. This IC uses a peak differential detector.
2. To adjust the detector coil, use the built-in automatic frequency circuit (AFC) and rotate the coil core until the voltage drop between pins 29 and 33 is 0 V.
3. Zeroing the AFC and minimizing the total harmonic distortion requires adjusting the capacitance between pin 30 and ground. Note that stray circuit board capacitance can affect this capacitance value.
4. The level of demodulation that is output depends on the inductance of the coil between pins 30 and 31, tuning capacity Q and the capacitor size. Note that although raising Q increases the slope of the S-curve and thus the demodulation output, it does so at the risk of increasing distortion.
5. If the destination market is Europe, increasing the slope of the S-curve helps reduce interference from neighboring channels.

IF Count Buffer

1. Pin 3 is the IF count buffer output. To activate the IF count circuit, apply a 5 V input to pin 3 through a 51 kΩ resistor.
2. The resistor connected to pin 2 determines the IF count buffer output sensitivity (seek stop sensitivity).
3. Leave pins 2 and 3 open if the IF count buffer is not used.
4. The largest time constant among those for the following pins determines the transient response characteristic of the IF count buffer.
Pin 1, the S-meter output, pin 4, the start of muting, pin 5, the muting drive output and pin 29, the AFC output.

IF count system block diagram

Unit (resistance: Ω, capacitance: F)

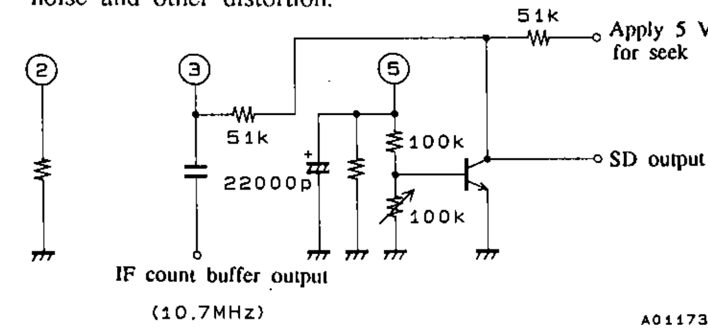


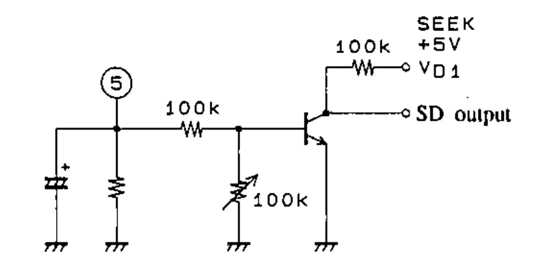
Note

The logical AND of the S-meter output and pin 3 control voltage generates the output 10.7 MHz IF count signal.

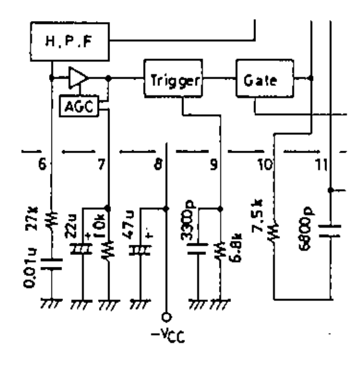
SD Output

1. To obtain SD output, attach an external NPN transistor to pin 5 as shown in the following figure.
2. The resistor connected between the base and ground is for adjusting the SD sensitivity.
3. The transient response characteristic of the resulting SD circuit on pin 5 is, like that for the IF count buffer, determined by the time constants for pins 1, 4, 5 and 29.
   Raising the seek speed requires decreasing the time constants. Decreasing them too far, however, reduces muting transient response and risks introducing beat noise and other distortion.





4. The following figure illustrates one possible circuit design using both the IF count buffer and the SD output circuit.



Unit (resistance: Ω, capacitance: F)

Noise Canceller Block

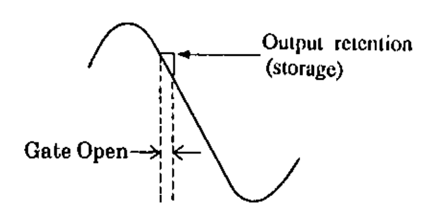
Noise canceller input waveform

PULSE NOISE

Gate Open

⟹

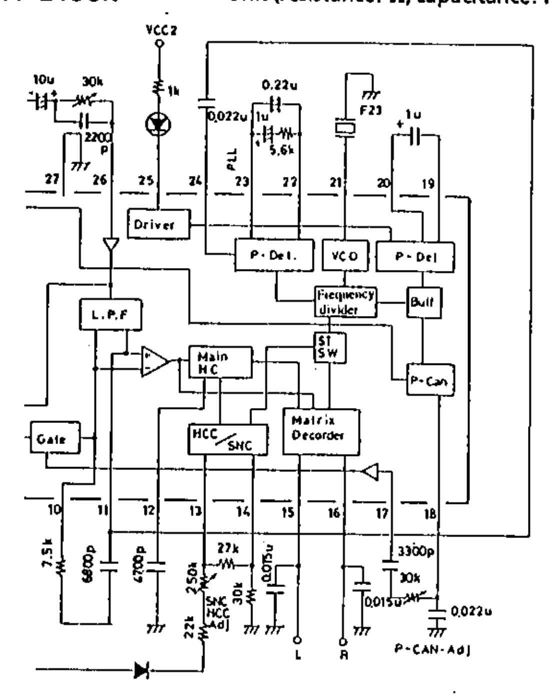
Noise canceller output waveform



1. The resistor and capacitor connected to pin 6 determine the noise canceller sensitivity.
2. The resistor and capacitor connected to pin 7 determine the noise AGC.
3. Pin 9 is the gate trigger output. The resistor and capacitor connected to pin 9 determine the length of time that the gate is open.
4. The resistor and capacitor connected to pins 10 and 11 are for holding the input signal level when the noise canceller gate operates. The storage time depends on the time that the gate is open. The time constant for the RC circuit on pins 10 and 11 must, therefore, be such that the output retention signal level does not drop during this interval.
5. Pin 26 is the noise canceller input. An appropriate input level is 250 mV_{rms} for 100% dev and f_m = 1 kHz. Excessive input can exceed the noise canceller dynamic range, increasing the THD. Insufficient input, on the other hand, lowers the signal-to-noise ratio and reduces pilot lamp sensitivity.

MPX Block

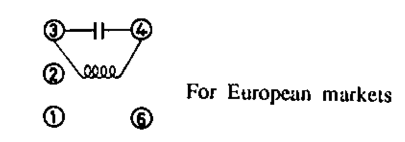
Unit (resistance: Ω, capacitance: F)



1. The variable resistor between pins 26 and 28 is for adjusting separation.
2. The ceramic oscillator must be a Murata F23. The use of other oscillators leads to frequency discrepancies and spurious oscillations.
3. Pin 14 is the SNC control input. It uses the S-meter output from pin 1 to automatically vary the stereo separation with the input signal strength. It is also possible to reduce noise resulting from weak stereo signals.
4. Pin 13 is the HCC control input. It uses the S-meter output from pin 1 to automatically vary the multiplexer output high-frequency characteristic with the input signal strength. The capacitor at pin 12 determines the maximum attenuation for this band. Too big a capacitance, however, will degrade music quality and make the audibility unstable during reception.
5. Pin 24 is the 19 kHz pilot signal input. Capacitively couple the 19 kHz component from pin 11 to pin 24.
6. Pin 25 is the stereo lamp signal. Current flows only for stereo signals. Leaving the pin open forces monaural operation.
7. The VCO always operates during both stereo and monaural operation.
8. Pins 15 and 16 are the left- and right-channel outputs. The capacitors at these pins determine the amount of deemphasis—50 µs using 0.015 µF, and 75 µs using 0.022 µF.
9. Pin 18 is the pilot cancel signal output. Adjust the variable resistor between pins 17 and 18 to minimize the 19 kHz pilot signal components in the left- and right-channel outputs for correct channel balance.
10. When adjusting the pilot cancel signal output, connect a 20 kHz lowpass filter (for example, a DIN audio filter) to the multiplexer output to remove the 38 kHz component and prevent its affect on the process of minimizing the 19 kHz component.
11. The capacitor connected to pin 34 is used to detect the pilot cancel signal. It should be connected to V_{CC} or GND. In the case of V_{CC}, use a capacitor with no DC leakage.

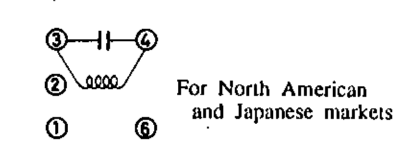
Coil Specifications

600YEAS-6889GW (Toko)



C=100p Internal

600YEAS-6890GW (Toko)



C=51p Internal

M7-T1-31301 (Mitsumi)

③ ④
② YD-0214
For European markets
① ⑥

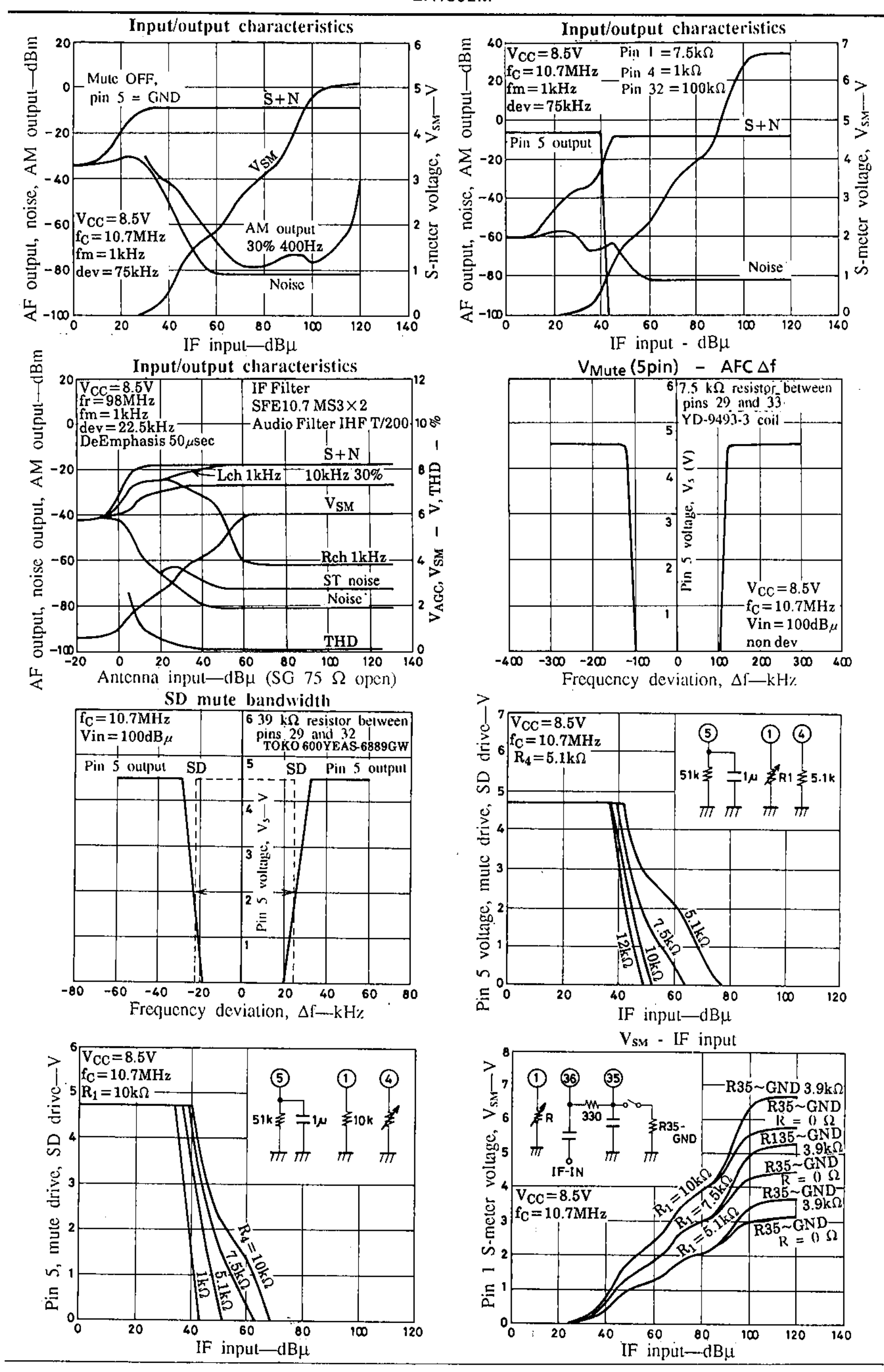
C=100p External

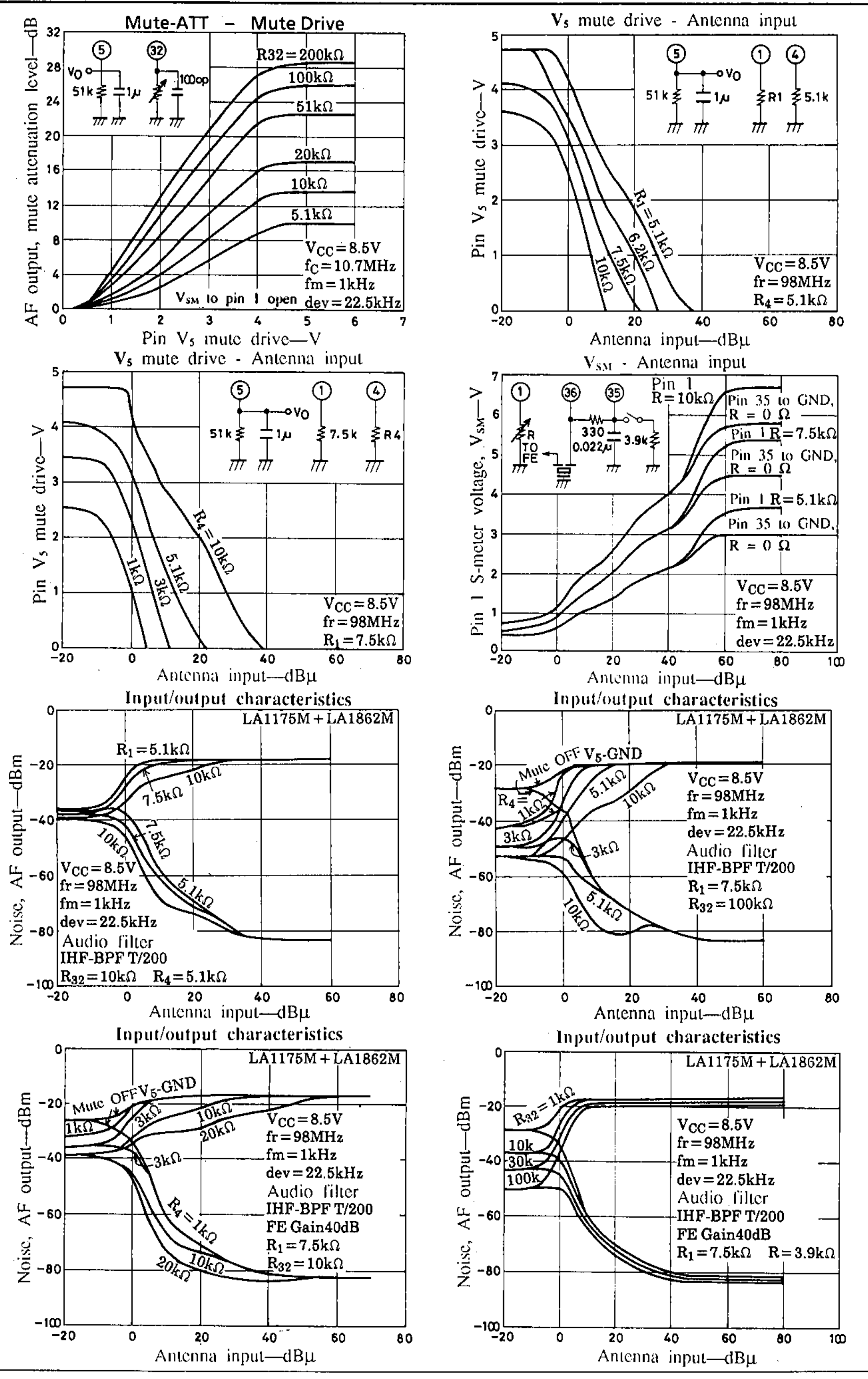
③ ④
② YD-9493-3
For North American and Japanese markets
① ⑥

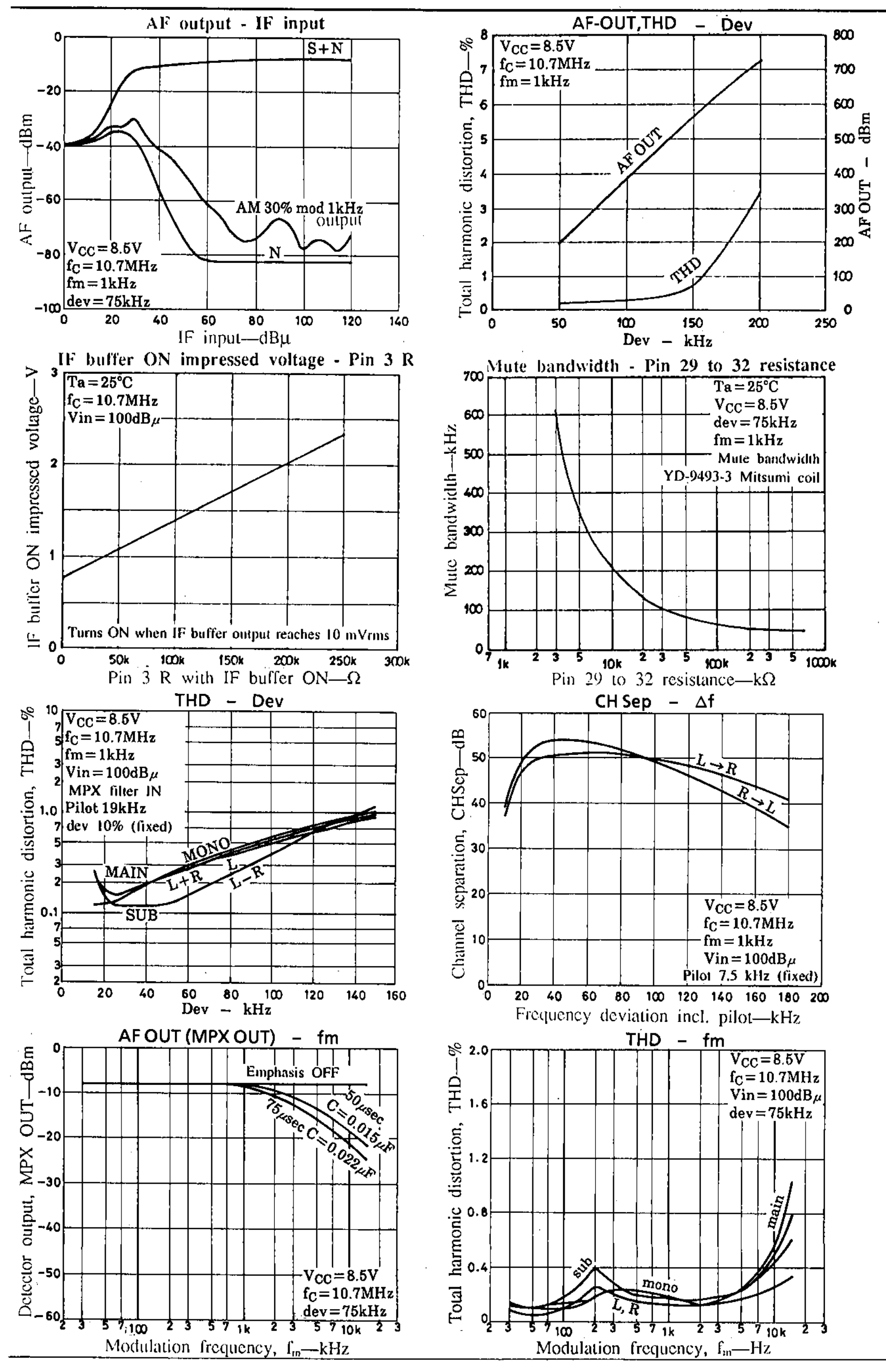
C=51p External

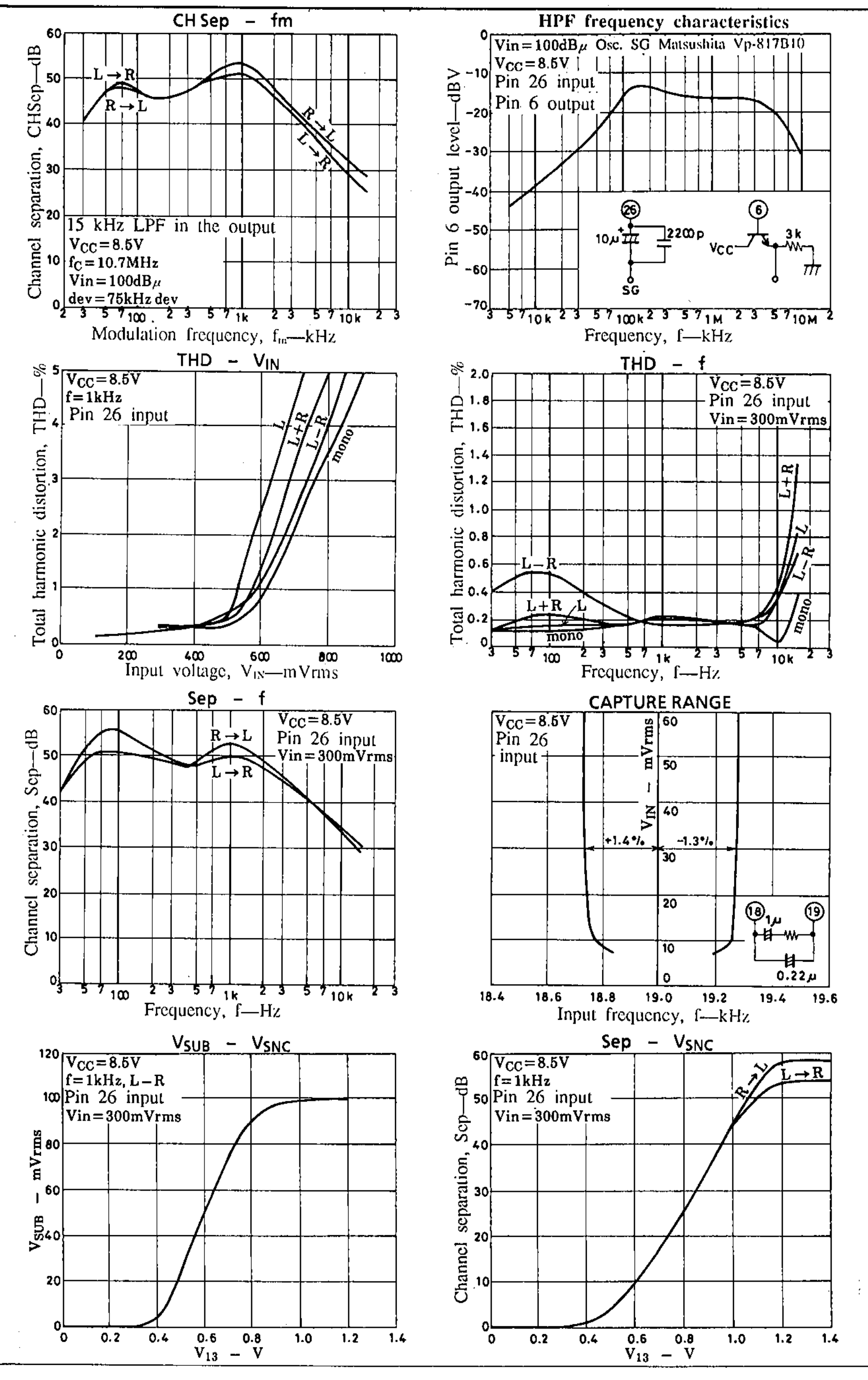
Note

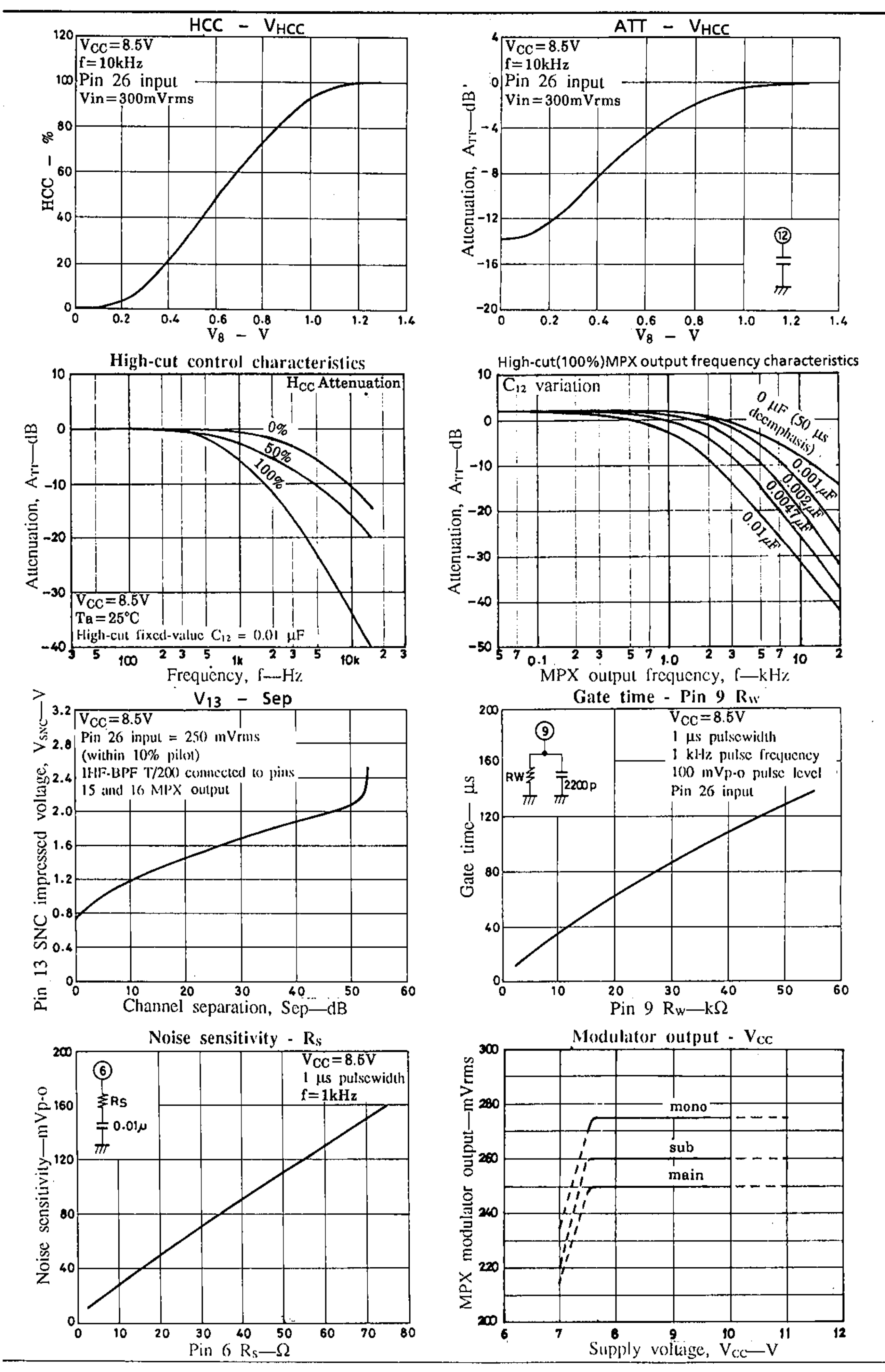
The dotted lines in the characteristics diagrams on the following pages represent device operation outside the device specifications.

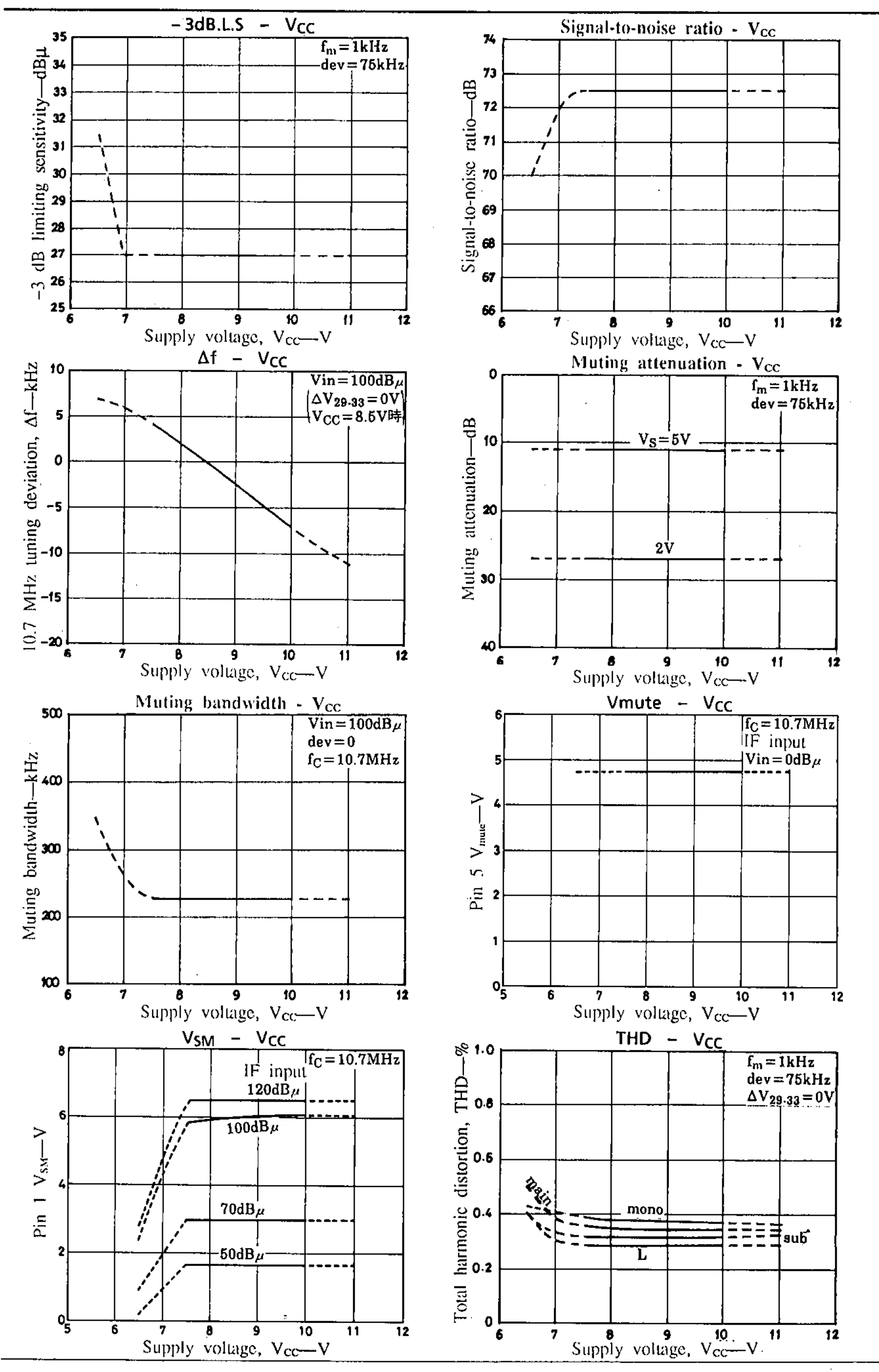

Input/output characteristics
Mute OFF, pin 5 = GND
S+N
VSM
AM output 30% 400Hz
Noise
VCC=8.5V
fC=10.7MHz
fm=1kHz
dev=75kHz
AF output, noise, AM output—dBm
S-meter voltage, VSM—V
IF input—dBμ
Input/output characteristics
VCC=8.5V
fC=10.7MHz
fm=1kHz
dev=75kHz
Pin 1 =7.5kΩ
Pin 4 =1kΩ
Pin 32 =100kΩ
Pin 5 output
S+N
Noise
IF input - dBμ
Input/output characteristics
VCC=8.5V
fr=98MHz
fm=1kHz
dev=22.5kHz
DeEmphasis 50μsec
IF Filter
SFE10.7 MS3×2
Audio Filter IHF T/200
S+N
Lch 1kHz
10kHz 30%
VSM
Rch 1kHz
ST noise
Noise
THD
VAGC, VSM — V, THD — %
Antenna input—dBμ (SG 75 Ω open)
VMute (5pin) - AFC Δf
7.5 kΩ resistor between pins 29 and 33
YD-9493-3 coil
Pin 5 voltage, Vs (V)
VCC=8.5V
fC=10.7MHz
Vin=100dBμ
non dev
Frequency deviation, Δf—kHz
SD mute bandwidth
fC=10.7MHz
Vin=100dBμ
39 kΩ resistor between pins 29 and 32
TOKO 600YEAS-6889GW
Pin 5 output
SD
Pin 5 voltage, Vs—V
Frequency deviation, Δf—kHz
VCC=8.5V
fC=10.7MHz
R4=5.1kΩ
51k
1μ
R1
5.1k
12kΩ
10kΩ
7.5kΩ
5.1kΩ
Pin 5 voltage, mute drive, SD drive—V
IF input—dBμ
VCC=8.5V
fC=10.7MHz
R1=10kΩ
51k
1μ
10k
1kΩ
5.1kΩ
7.5kΩ
R4=10kΩ
Pin 5, mute drive, SD drive—V
IF input—dBμ
VSM - IF input
R
330
R35-GND
IF-IN
VCC=8.5V
fC=10.7MHz
R35~GND 3.9kΩ
R35~GND R = 0 Ω
R135~GND 3.9kΩ
R35~GND R = 0 Ω
R35~GND 3.9kΩ
R35~GND R = 0 Ω
R1=10kΩ
R1=7.5kΩ
R1=5.1kΩ
Pin 1 S-meter voltage, VSM—V
IF input—dBμ

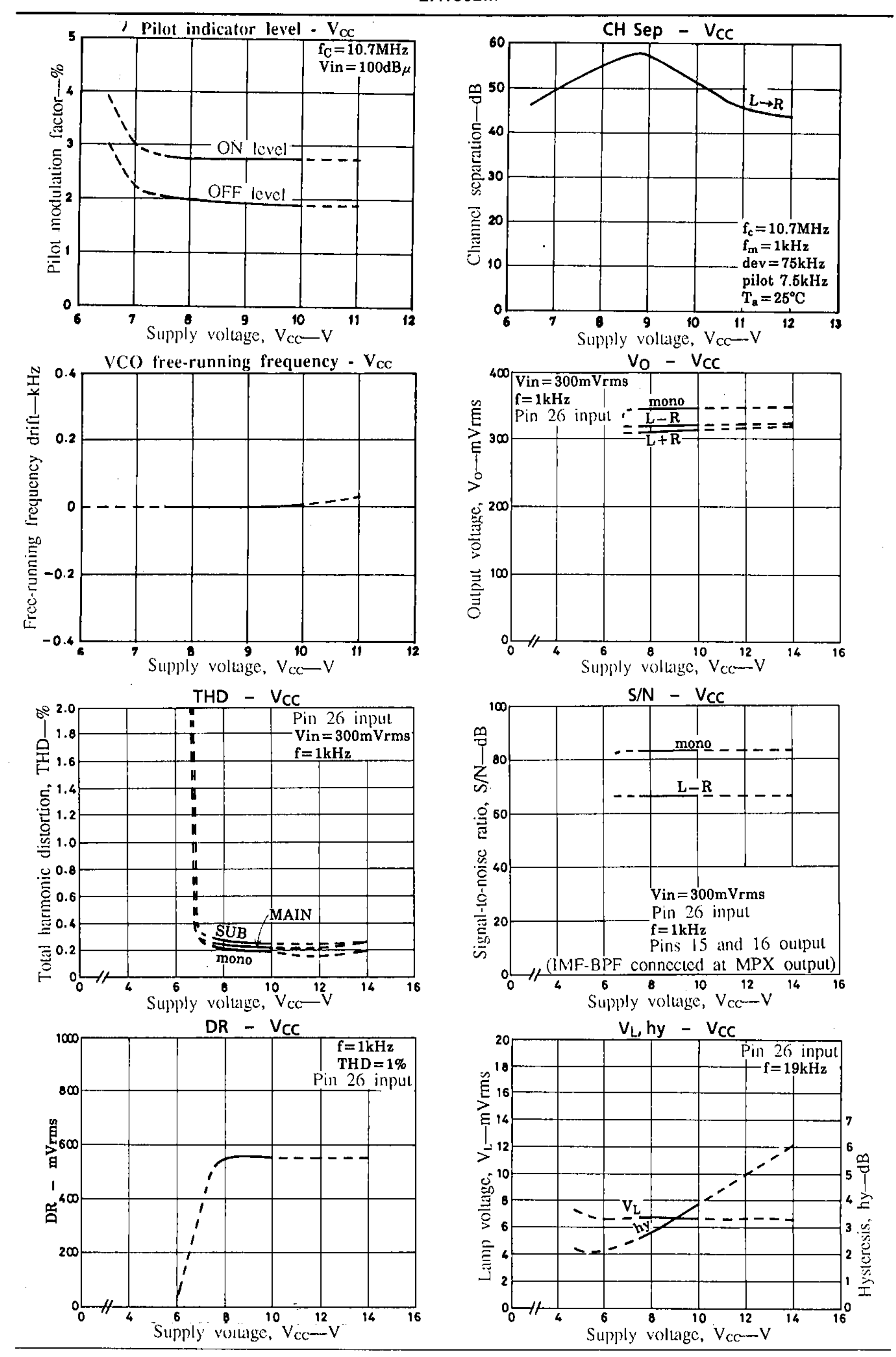

Mute-ATT – Mute Drive
AF output, mute attenuation level—dB
Pin V5 mute drive—V
R32=200kΩ
100kΩ
51kΩ
20kΩ
10kΩ
5.1kΩ
VCC=8.5V
fC=10.7MHz
fm=1kHz
dev=22.5kHz
VSM to pin 1 open
V5 mute drive - Antenna input
Pin V5 mute drive—V
Antenna input—dBμ
R1=5.1kΩ
6.2kΩ
7.5kΩ
10kΩ
VCC=8.5V
fr=98MHz
R4=5.1kΩ
V5 mute drive - Antenna input
R4=10kΩ
5.1kΩ
3kΩ
1kΩ
VCC=8.5V
fr=98MHz
R1=7.5kΩ
VSM - Antenna input
Pin 1 S-meter voltage, VSM—V
Pin 1 R=10kΩ
Pin 35 to GND, R = 0 Ω
Pin 1 R=7.5kΩ
Pin 35 to GND, R = 0 Ω
Pin 1 R=5.1kΩ
Pin 35 to GND, R = 0 Ω
VCC=8.5V
fr=98MHz
fm=1kHz
dev=22.5kHz
Input/output characteristics
Noise, AF output—dBm
LA1175M+LA1862M
R1=5.1kΩ
7.5kΩ 10kΩ
10kΩ
7.5kΩ
5.1kΩ
VCC=8.5V
fr=98MHz
fm=1kHz
dev=22.5kHz
Audio filter
IHF-BPF T/200
R32=10kΩ R4=5.1kΩ
Input/output characteristics
LA1175M+LA1862M
Mute OFF V5-GND
R4=1kΩ
3kΩ
5.1kΩ
10kΩ
VCC=8.5V
fr=98MHz
fm=1kHz
dev=22.5kHz
Audio filter
IHF-BPF T/200
R1=7.5kΩ
R32=100kΩ
Input/output characteristics
LA1175M+LA1862M
Mute OFF V5-GND
1kΩ
3kΩ
10kΩ
20kΩ
R4=1kΩ
VCC=8.5V
fr=98MHz
fm=1kHz
dev=22.5kHz
Audio filter
IHF-BPF T/200
FE Gain40dB
R1=7.5kΩ
R32=10kΩ
Input/output characteristics
LA1175M+LA1862M
R32=1kΩ
10k
30k
100k
VCC=8.5V
fr=98MHz
fm=1kHz
dev=22.5kHz
Audio filter
IHF-BPF T/200
FE Gain40dB
R1=7.5kΩ R=3.9kΩ
Antenna input—dBμ

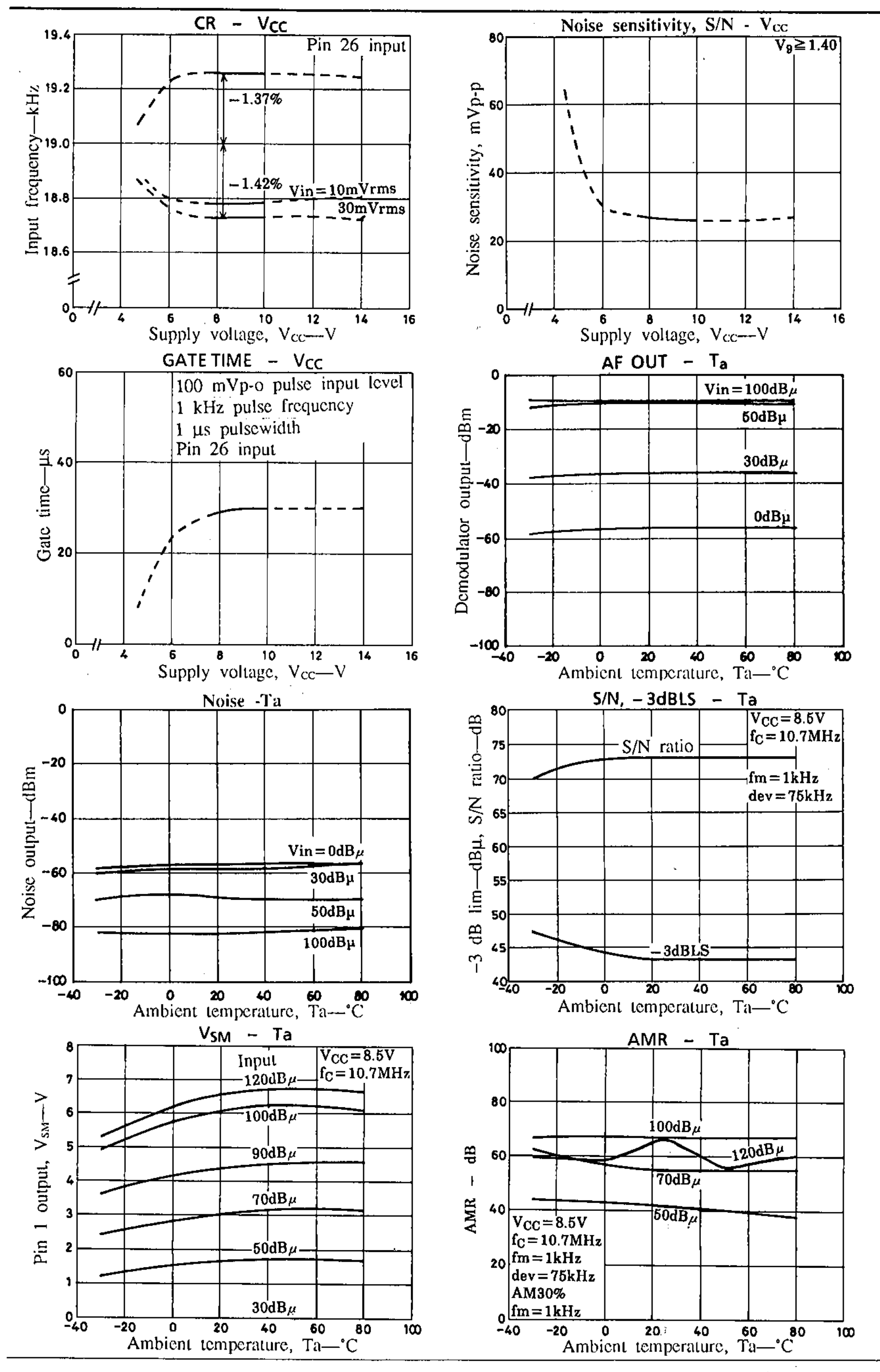

AF output - IF input
S+N
AM 30% mod 1kHz output
N
VCC=8.5V
fC=10.7MHz
fm=1kHz
dev=75kHz
AF output—dBm
IF input—dBμ
AF-OUT,THD - Dev
VCC=8.5V
fC=10.7MHz
fm=1kHz
AF OUT
THD
Total harmonic distortion, THD—%
AF OUT - dBm
Dev - kHz
IF buffer ON impressed voltage - Pin 3 R
Ta=25°C
fC=10.7MHz
Vin=100dBμ
Turns ON when IF buffer output reaches 10 mVrms
IF buffer ON impressed voltage—V
Pin 3 R with IF buffer ON—Ω
Mute bandwidth - Pin 29 to 32 resistance
Ta=25°C
VCC=8.5V
dev=75kHz
fm=1kHz
Mute bandwidth
YD-9493-3 Mitsumi coil
Mute bandwidth—kHz
Pin 29 to 32 resistance—kΩ
THD - Dev
VCC=8.5V
fC=10.7MHz
fm=1kHz
Vin=100dBμ
MPX filter IN
Pilot 19kHz
dev 10% (fixed)
MONO
MAIN
L+R
L
L-R
SUB
Total harmonic distortion, THD—%
Dev - kHz
CH Sep - Δf
L→R
R→L
VCC=8.5V
fC=10.7MHz
fm=1kHz
Vin=100dBμ
Pilot 7.5 kHz (fixed)
Channel separation, CHSep—dB
Frequency deviation incl. pilot—kHz
AF OUT (MPX OUT) - fm
Emphasis OFF
50μsec C=0.015μF
75μsec C=0.022μF
VCC=8.5V
fC=10.7MHz
dev=75kHz
Detector output, MPX OUT—dBm
Modulation frequency, fm—kHz
THD - fm
VCC=8.5V
fC=10.7MHz
Vin=100dBμ
dev=75kHz
main
sub
mono
L, R
Total harmonic distortion, THD—%
Modulation frequency, fm—Hz


CH Sep – fm
L→R
R→L
R→L
L→R
15 kHz LPF in the output
VCC=8.5V
fC=10.7MHz
Vin=100dBμ
dev=75kHz dev
Channel separation, CHSep—dB
Modulation frequency, fm—kHz
HPF frequency characteristics
Vin=100dBμ Osc. SG Matsushita Vp-817B10
VCC=8.5V
Pin 26 input
Pin 6 output
10μ
2200p
SG
Vcc
3k
Pin 6 output level—dBV
Frequency, f—kHz
THD – VIN
VCC=8.5V
f=1kHz
Pin 26 input
L
L+R
L–R
mono
Total harmonic distortion, THD—%
Input voltage, VIN—mVrms
THD – f
VCC=8.5V
Pin 26 input
Vin=300mVrms
L–R
L+R
L
mono
Total harmonic distortion, THD—%
Frequency, f—Hz
Sep – f
VCC=8.5V
Pin 26 input
Vin=300mVrms
R→L
L→R
Channel separation, Sep—dB
Frequency, f—Hz
CAPTURE RANGE
VCC=8.5V
Pin 26
input
VIN – mVrms
+1.4%
-1.3%
1μ
0.22μ
Input frequency, f—kHz
VSUB – VSNC
VCC=8.5V
f=1kHz, L–R
Pin 26 input
Vin=300mVrms
VSUB – mVrms
V13 – V
Sep – VSNC
VCC=8.5V
f=1kHz
Pin 26 input
Vin=300mVrms
R→L
L→R
Channel separation, Sep—dB
V13 – V

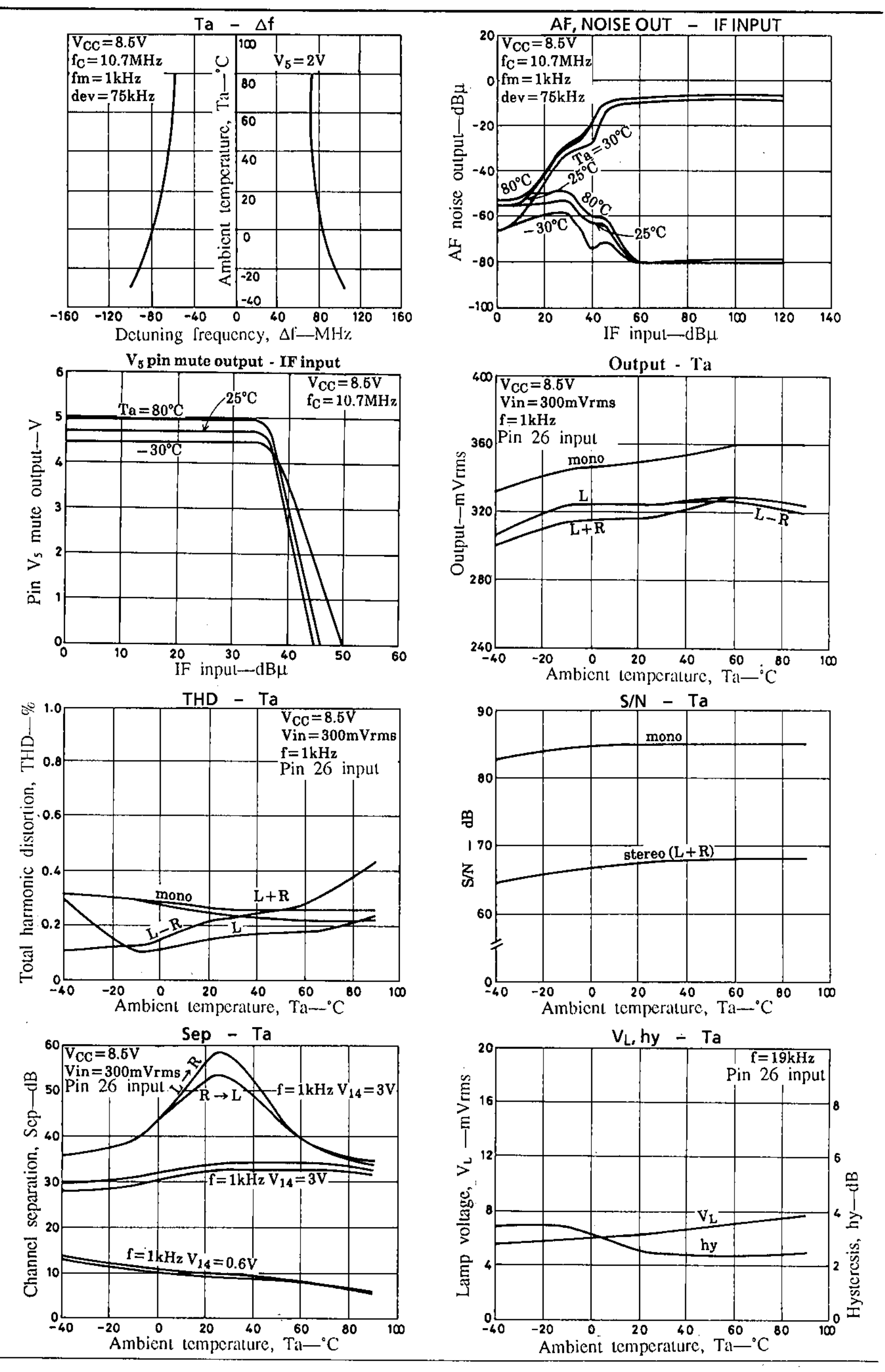

HCC – VHCC
VCC=8.5V
f=10kHz
Pin 26 input
Vin=300mVrms
HCC – %
V8 – V
ATT – VHCC
Attenuation, ATT—dB
High-cut control characteristics
HCC Attenuation
0%
50%
100%
VCC=8.5V
Ta=25°C
High-cut fixed-value C12 = 0.01 μF
Frequency, f—Hz
High-cut(100%)MPX output frequency characteristics
C12 variation
0 μF (50 μs deemphasis)
0.001μF
0.002μF
0.0047μF
0.01μF
MPX output frequency, f—kHz
V13 – Sep
Pin 26 input = 250 mVrms
(within 10% pilot)
IHF-BPF T/200 connected to pins
15 and 16 MPX output
Pin 13 SNC impressed voltage, VSNC—V
Channel separation, Sep—dB
Gate time - Pin 9 Rw
1 μs pulsewidth
1 kHz pulse frequency
100 mVp-o pulse level
Pin 26 input
RW
2200p
Gate time— μs
Pin 9 Rw—kΩ
Noise sensitivity - Rs
f=1kHz
Rs
0.01μ
Noise sensitivity—mVp-o
Pin 6 Rs—Ω
Modulator output - Vcc
mono
sub
main
MPX modulator output—mVrms
Supply voltage, Vcc—V

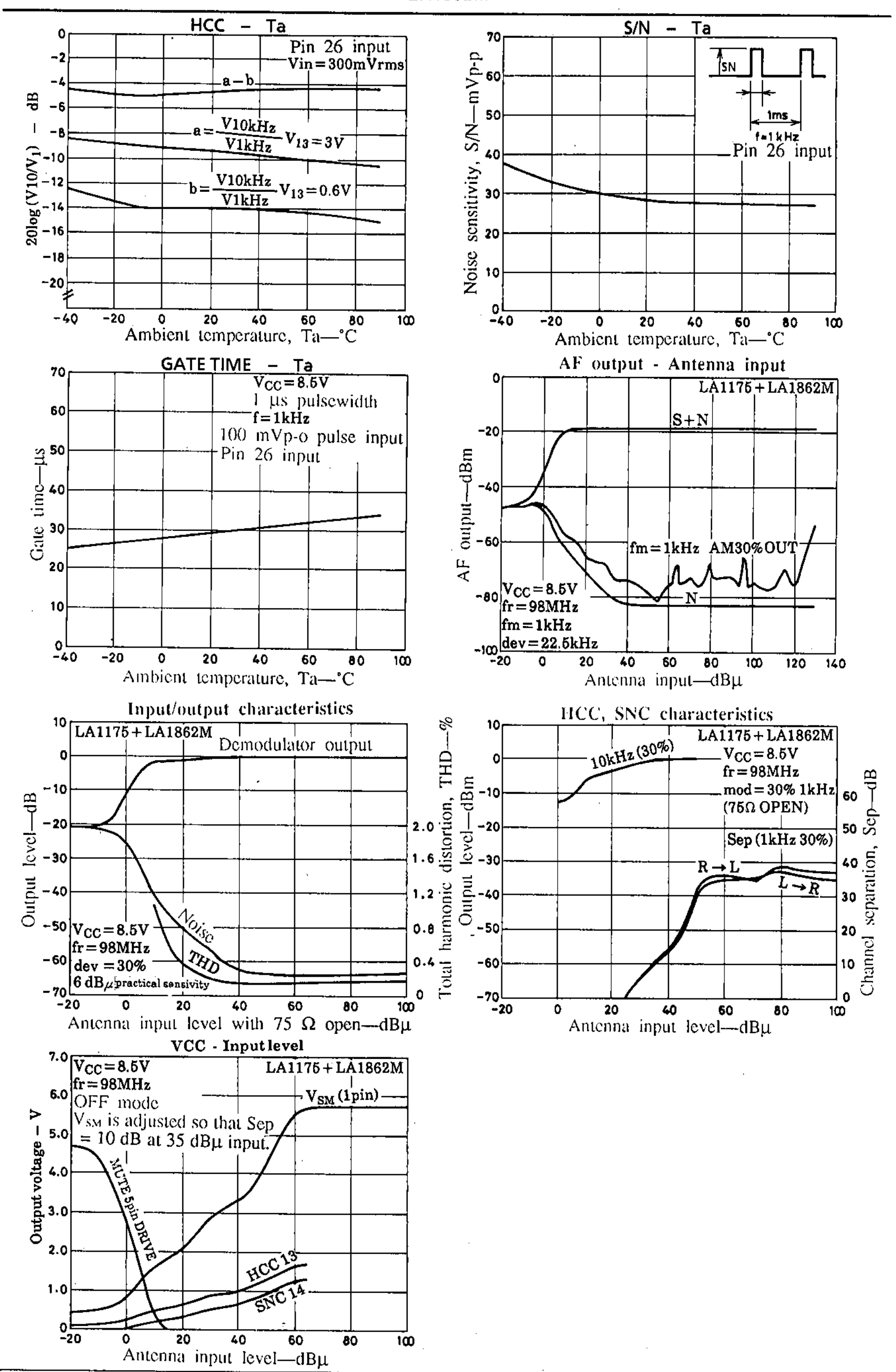

-3dB.L.S - Vcc
fm=1kHz
dev=75kHz
-3 dB limiting sensitivity—dBμ
Supply voltage, Vcc—V
Signal-to-noise ratio - Vcc
Signal-to-noise ratio—dB
Supply voltage, Vcc—V
Δf - Vcc
Vin=100dBμ
(ΔV29-33=0V)
(Vcc=8.5V時)
10.7 MHz tuning deviation, Δf—kHz
Supply voltage, Vcc—V
Muting attenuation - Vcc
fm=1kHz
dev=75kHz
VS=5V
2V
Muting attenuation—dB
Supply voltage, Vcc—V
Muting bandwidth - Vcc
Vin=100dBμ
dev=0
fC=10.7MHz
Muting bandwidth—kHz
Supply voltage, Vcc—V
Vmute - Vcc
fC=10.7MHz
IF input
Vin=0dBμ
Pin 5 Vmute—V
Supply voltage, Vcc—V
VSM - Vcc
fC=10.7MHz
IF input
120dBμ
100dBμ
70dBμ
50dBμ
Pin 1 VSM—V
Supply voltage, Vcc—V
THD - Vcc
fm=1kHz
dev=75kHz
ΔV29-33=0V
main
mono
sub
L
Total harmonic distortion, THD—%
Supply voltage, Vcc—V


Pilot indicator level - V_{CC}
f_C=10.7MHz
Vin=100dBμ
ON level
OFF level
Pilot modulation factor—%
Supply voltage, V_{CC}—V
CH Sep - V_{CC}
L→R
f_c=10.7MHz
f_m=1kHz
dev=75kHz
pilot 7.5kHz
T_a=25°C
Channel separation—dB
Supply voltage, V_{CC}—V
VCO free-running frequency - V_{CC}
Free-running frequency drift—kHz
Supply voltage, V_{CC}—V
V_O - V_{CC}
Vin=300mVrms
f=1kHz
Pin 26 input
mono
L−R
L+R
Output voltage, V_O—mVrms
Supply voltage, V_{CC}—V
THD - V_{CC}
Pin 26 input
Vin=300mVrms
f=1kHz
MAIN
SUB
mono
Total harmonic distortion, THD—%
Supply voltage, V_{CC}—V
S/N - V_{CC}
mono
L−R
Vin=300mVrms
Pin 26 input
f=1kHz
Pins 15 and 16 output
(IMF-BPF connected at MPX output)
Signal-to-noise ratio, S/N—dB
Supply voltage, V_{CC}—V
DR - V_{CC}
f=1kHz
THD=1%
Pin 26 input
DR - mVrms
Supply voltage, V_{CC}—V
V_L, hy - V_{CC}
Pin 26 input
f=19kHz
V_L
hy
Lamp voltage, V_L—mVrms
Hysteresis, hy—dB
Supply voltage, V_{CC}—V



CR - VCC
Pin 26 input
−1.37%
−1.42%
Vin=10mVrms
30mVrms
Input frequency—kHz
Supply voltage, VCC—V
Noise sensitivity, S/N - VCC
V9≧1.40
Noise sensitivity, mVp-p
Supply voltage, VCC—V
GATE TIME - VCC
100 mVp-o pulse input level
1 kHz pulse frequency
1 μs pulsewidth
Pin 26 input
Gate time—μs
Supply voltage, VCC—V
AF OUT - Ta
Vin=100dBμ
50dBμ
30dBμ
0dBμ
Demodulator output—dBm
Ambient temperature, Ta—°C
Noise -Ta
Vin=0dBμ
30dBμ
50dBμ
100dBμ
Noise output—dBm
Ambient temperature, Ta—°C
S/N, −3dBLS - Ta
VCC=8.5V
fC=10.7MHz
S/N ratio
fm=1kHz
dev=75kHz
−3dBLS
−3 dB lim—dBμ, S/N ratio—dB
Ambient temperature, Ta—°C
VSM - Ta
Input
VCC=8.5V
fC=10.7MHz
120dBμ
100dBμ
90dBμ
70dBμ
50dBμ
30dBμ
Pin 1 output, VSM—V
Ambient temperature, Ta—°C
AMR - Ta
100dBμ
120dBμ
70dBμ
50dBμ
VCC=8.5V
fC=10.7MHz
fm=1kHz
dev=75kHz
AM30%
fm=1kHz
AMR - dB
Ambient temperature, Ta—°C


Ta - Δf
VCC=8.5V
fC=10.7MHz
fm=1kHz
dev=75kHz
V5=2V
Ambient temperature, Ta—°C
Detuning frequency, Δf—MHz
AF, NOISE OUT - IF INPUT
Ta=30°C
25°C
80°C
-30°C
AF noise output—dBμ
IF input—dBμ
V5 pin mute output - IF input
fC=10.7MHz
Ta=80°C
Pin V5 mute output—V
Output - Ta
Vin=300mVrms
f=1kHz
Pin 26 input
mono
L
L+R
L-R
Output—mVrms
THD - Ta
Total harmonic distortion, THD—%
S/N - Ta
stereo (L+R)
S/N - dB
Sep - Ta
L→R
R→L
f=1kHz V14=3V
f=1kHz V14=0.6V
Channel separation, Sep—dB
VL, hy - Ta
f=19kHz
VL
hy
Lamp voltage, VL —mVrms
Hysteresis, hy—dB
Ambient temperature, Ta—°C


HCC - Ta
Pin 26 input
Vin=300mVrms
a−b
a = V10kHz / V1kHz V13=3V
b = V10kHz / V1kHz V13=0.6V
20log (V10/V1) − dB
Ambient temperature, Ta—°C
S/N - Ta
SN
1ms
f=1kHz
Pin 26 input
Noise sensitivity, S/N—mVp-p
Ambient temperature, Ta—°C
GATE TIME - Ta
VCC=8.5V
1 µs pulsewidth
f=1kHz
100 mVp-o pulse input
Pin 26 input
Gate time—µs
Ambient temperature, Ta—°C
AF output - Antenna input
LA1175+LA1862M
S+N
fm=1kHz AM30%OUT
N
VCC=8.5V
fr=98MHz
fm=1kHz
dev=22.5kHz
AF output—dBm
Antenna input—dBµ
Input/output characteristics
LA1175+LA1862M
Demodulator output
Noise
THD
VCC=8.5V
fr=98MHz
dev =30%
6 dBµ practical sensivity
Output level—dB
Total harmonic distortion, THD—%
Antenna input level with 75 Ω open—dBµ
HCC, SNC characteristics
LA1175+LA1862M
10kHz (30%)
VCC=8.5V
fr=98MHz
mod=30% 1kHz
(75Ω OPEN)
Sep (1kHz 30%)
R→L
L→R
Output level—dBm
Channel separation, Sep—dB
Antenna input level—dBµ
VCC - Input level
VCC=8.5V
fr=98MHz
OFF mode
VSM is adjusted so that Sep = 10 dB at 35 dBµ input.
LA1175+LA1862M
VSM (1pin)
MUTE 5pin DRIVE
HCC 13
SNC 14
Output voltage – V
Antenna input level—dBµ